IN THE CLAIMS

Kindly cancel claims 2, 12, 16 and 18 without prejudice, add new claim 19, and amend claims 4, 5, 6, 11, and 13 as shown in the following claim listing:

1. (canceled)

2. (canceled)

3. (canceled)

4. (currently amended) The timing recovery loop as recited in claim ~~3~~ 19, further comprising ~~a~~ finite impulse response (FIR) ~~filter~~ filters electrically coupling the carrier recovery ~~circuit~~ circuits to the forward ~~equalizer~~ equalizers.

5. (currently amended) The timing recovery loop as recited in claim 4, wherein the FIR ~~filter~~ filters ~~is a~~ are square-root raised cosine ~~filter~~ filters.

6. (currently amended) A digital receiver connected to N antennae including N timing recovery loops electrically coupled to the N antennae, each of the N timing recovery loops constructed as recited in claim ~~2~~ 7.

7. (previously presented) A timing recovery loop in the front end of a digital receiver including N antennae, comprising:

N sample rate converters each receiving an Nth symbol stream at a first sampling rate from an Nth antenna and outputs the Nth

symbol stream at a second sampling rate responsive to a timing recovery (TR) control signal;

N forward equalizers generating an Nth equalized feedback signal based on the Nth symbol stream at the second sampling rate, respectively; and

a timing recovery circuit generating the TR control signal based upon the N equalized feedback signals.

8.(original) The timing recovery loop as recited in claim 7, further comprising N carrier recovery circuits, each electrically coupling an Nth one of the N sample rate converters to an Nth one of the forward equalizers.

9.(original) The timing recovery loop as recited in claim 8, further comprising N finite impulse response (FIR) filters, each electrically coupling an Nth one of the carrier recovery circuits to an Nth one of the forward equalizers.

10. (original) The timing recovery loop as recited in claim 9, wherein each of the N FIR filters is a square-root raised cosine filter.

11. (currently amended) A timing recovery loop in the front end of a digital receiver including N antennae, comprising:

N sample rate converters, each receiving an Nth symbol stream at a first sampling rate from an Nth antenna and outputting the Nth symbol stream at a second sampling rate responsive to a timing recovery (TR) control signal;

N forward equalizers, each generating an Nth equalized feedback signal based on the Nth symbol stream at the second sampling rate, respectively; ~~and~~

a timing recovery circuit generating the TR control signal based upon a selected one of the N equalized feedback signals~~.~~ ; and N carrier recovery circuits, each electrically coupling an Nth one of the N sample rate converters to an Nth one of the forward equalizers.

12.(canceled)

13. (currently amended)The timing recovery loop as recited in claim ~~12~~ 11, further comprising N finite impulse response (FIR) filters, each electrically coupling an Nth one of the carrier recovery circuits to an Nth one of the forward equalizers.

14.(original) The timing recovery loop as recited in claim 13, wherein each of the N FIR filters is a square-root raised cosine filter.

15.(original) The timing recovery loop as recited in claim 11, further comprising a selector receiving N signals based on the N equalized feedback signals at N respective input terminals and applying the selected one of the N signals to the timing recovery circuit.

16.(cancelled)

17. (previously presented) A method for operating a digital receiver, including N sample rate converters responsive to a timing recovery (TR) control signal, connected to N antennae, respectively, comprising:

generating N equalized feedback signals, each based on an Nth symbol stream having a controlled sample rate;

combining the N equalized feedback signal to produce a combined equalized feedback signal;

producing the TR control signal based on the combined equalized feedback signal; and

applying the TR control signal to the sample rate converters to thereby permit the N sample rate converters to output N symbol streams at the controlled sample rate.

18.(cancelled)

Add new claim 19.

19. (New) The timing recovery loop as recited in claim 7, further comprising carrier recovery circuits electrically coupling the sample rate converters to the forward equalizers.